

6-18GHz 4 bit Digital Variable Amplifier

GaAs Monolithic Microwave IC

Description

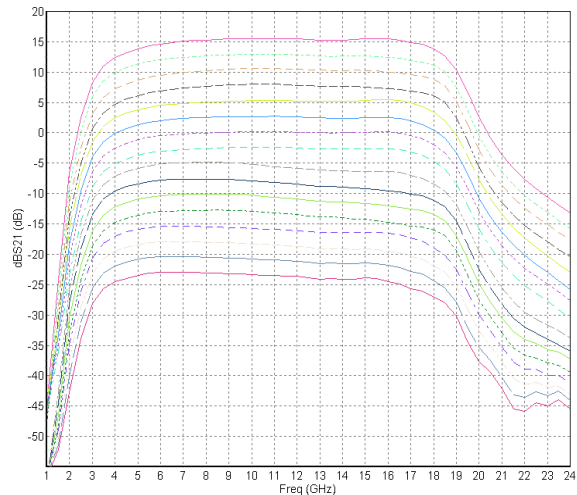
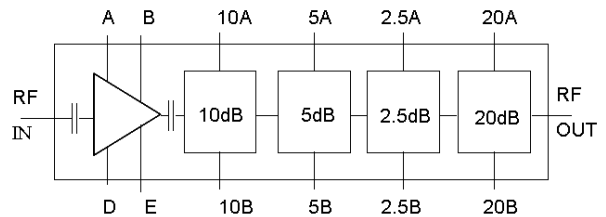
The CHA3514 is composed by a two stage travelling wave amplifier followed by a four steps digital attenuator. It is designed for defense applications. The backside of the chip is both RF and DC grounded. This helps to simplify the assembly process.

The circuit is manufactured with a pHEMT process, 0.25 μ m gate length, via holes through the substrate, air bridges and electron beam gate lithography.

It is available in chip form.

Main Features

- Performances: 6-18GHz
- 19dBm saturated output power
- 13 dB gain
- 4bit attenuator for 39.5dB dynamic range
- DC power consumption, 190mA @ 4.5V
- Chip size: 5.54 x 2.30 x 0.1mm



Typical on wafer Measurements
Gain versus attenuation states

Main Characteristics

Tamb. = 25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	6		18	GHz
G	Small signal gain @ Attenuator state 0dB		13		dB
Psat	Saturated Output power @ Attenuator state 0dB		19		dBm
ATT dyn	Attenuator range with 4bit		39.5		dB

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions!

Electrical Characteristics on wafer

Tamb = +25°C

Vd = Pads B, D = 4.5V, Vg = Pads A, E tuned for Id = 190mA

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range (1)	6		18	GHz
G	Small signal gain @ Attenuator state 0dB (1)	11	13		dB
ATT bit	Attenuator bit: State 2.5dB	2	2.6	3.5	dB
	State 5dB	4	5	6	dB
	State 10 dB	9	10	11	dB
	State 20dB	19	22	23	dB
ATT dyn	Attenuator dynamic range with 4bit	35	39.5		dB
P1dB	Output power at 1dB compression @ Attenuator state 0dB (1)		18		dBm
Psat	Saturated Output power @ Attenuator state 0dB (1)		19		dBm
NF	Noise figure @ Attenuator state 0dB		7		dB
RL_IN	Input Return Loss all attenuator states		-13	-8	dB
RL_OUT	Output Return Loss all attenuator states		-15	-9	dB
Vd	Drain bias DC voltage (Pads B,D)		4.5		V
Id	Bias current @ small signal		190	250	mA
Vc	Control voltage for Attenuator bits	-5		0	V

(1) These values are representative for on-wafer measurements that are made without bonding wires at the RF ports.

Absolute Maximum Ratings

Tamb. = 25°C (1)

Symbol	Parameter	Values	Unit
Vd	Maximum Drain bias voltage (Pads B,D)	+5	V
Id	Drain bias current with Vd=4.5V	320	mA
Vg	Gate bias voltage (Pads A, E)	-2 to +0.4	V
Vc	Attenuator bits control voltage	-7 to +0.6	V
Pin	Maximum input power overdrive (2)	+20.0	dBm
Tch	Maximum channel temperature	+175	°C
Ta	Operating temperature range	-40 to +70	°C
Tstg	Storage temperature range	-55 to +125	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

(2) Duration < 1s.

4bit VGA Control interface

The attenuator states are controlled by 8 voltages.

state	Theoretical attenuation dB	Voltage CONTROL PAD							
		10A (V)	10B (V)	5A (V)	5B (V)	2.5A (V)	2.5B (V)	20A (V)	20B (V)
0	0 référence	-5	0	-5	0	-5	0	-5	0
1	2.5	-5	0	-5	0	0	-5	-5	0
2	5	-5	0	0	-5	-5	0	-5	0
3	7.5	-5	0	0	-5	0	-5	-5	0
4	10	0	-5	-5	0	-5	0	-5	0
5	12.5	0	-5	-5	0	0	-5	-5	0
6	15	0	-5	0	-5	-5	0	-5	0
7	17.5	0	-5	0	-5	0	-5	-5	0
8	20	-5	0	-5	0	-5	0	0	-5
9	22.5	-5	0	-5	0	0	-5	0	-5
10	25	-5	0	0	-5	-5	0	0	-5
11	27.5	-5	0	0	-5	0	-5	0	-5
12	30	0	-5	-5	0	-5	0	0	-5
13	32.5	0	-5	-5	0	0	-5	0	-5
14	35	0	-5	0	-5	-5	0	0	-5
15	37.5	0	-5	0	-5	0	-5	0	-5

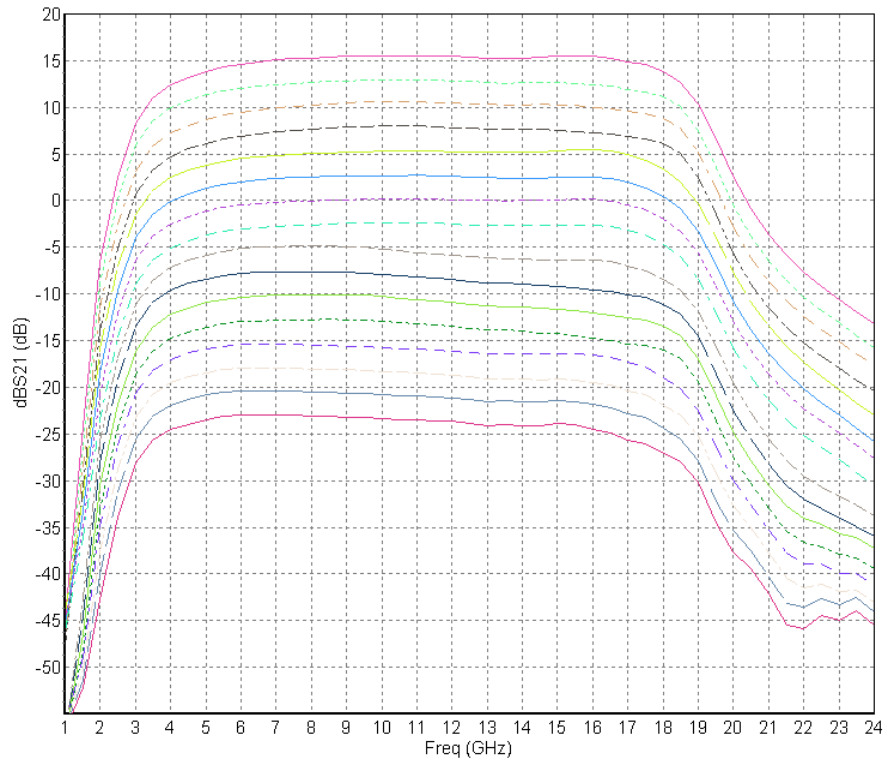
Typical chip on wafer Sij parameters for reference state

Tamb 25°C, B = D = 4.5V, Id = 190mA, 10A, 5A, 2.5A, 20A = -5V, 10B, 5B, 2.5B, 20B = 0V

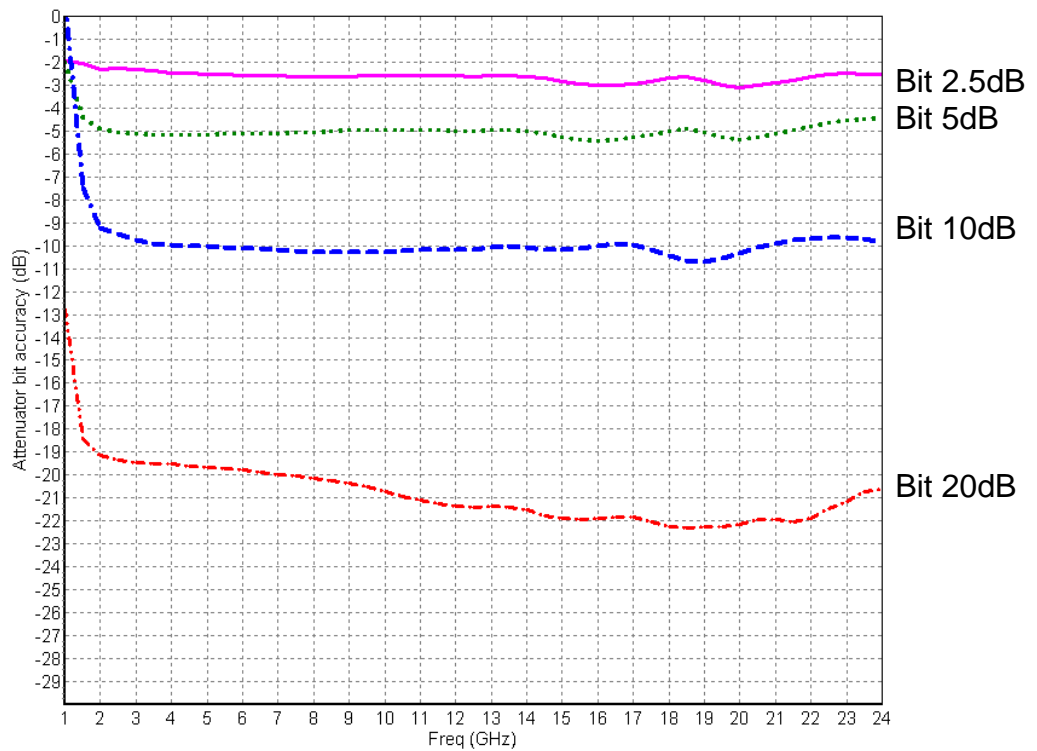
Freq (GHz)	dB(S11)	P(S11) (°)	dB(S21)	P(S21) (°)	dB(S12)	P(S12) (°)	dB(S22)	P(S22) (°)
1.0	-0.8	-42.4	-44.8	-114.9	-69.9	-91.3	-3.3	-59.4
1.5	-1.5	-62.3	-24.1	-166.4	-69.2	-148.8	-4.6	-89.6
2.0	-2.1	-81.0	-6.6	156.9	-67.0	-165.4	-7.2	-122.7
2.5	-2.8	-99.6	2.5	94.4	-61.4	-179.5	-10.5	-160.5
3.0	-4.1	-116.9	8.3	37.6	-69.4	74.2	-14.8	147.5
3.5	-5.1	-133.6	11.0	-17.7	-86.1	97.0	-17.4	88.8
4.0	-6.3	-148.7	12.4	-65.1	-78.4	133.3	-16.9	43.1
4.5	-7.8	-162.3	13.3	-107.0	-72.8	112.9	-15.5	15.9
5.0	-9.3	-175.1	13.9	-145.1	-70.0	77.8	-14.4	-2.5
5.5	-10.7	174.7	14.3	178.9	-68.7	34.4	-13.5	-17.5
6.0	-12.2	167.3	14.6	144.5	-66.8	-5.4	-12.9	-30.6
6.5	-13.8	161.4	14.9	111.4	-64.9	-37.6	-12.4	-42.3
7.0	-15.0	157.0	15.1	79.3	-67.2	-61.6	-12.1	-54.0
7.5	-15.6	155.3	15.2	47.9	-62.7	-85.6	-12.0	-66.0
8.0	-16.2	156.1	15.3	16.9	-59.7	-109.9	-12.2	-78.5
8.5	-16.6	154.3	15.4	-13.7	-57.5	-138.0	-12.7	-90.1
9.0	-16.1	151.1	15.5	-44.0	-55.6	-167.3	-13.6	-102.2
9.5	-15.3	148.6	15.5	-73.9	-54.7	171.2	-15.1	-113.3
10.0	-14.6	145.0	15.5	-103.8	-53.2	136.4	-17.3	-123.0
10.5	-14.0	136.7	15.5	-133.5	-54.7	117.6	-20.4	-125.3
11.0	-13.0	127.2	15.5	-163.1	-56.0	96.6	-23.7	-113.1
11.5	-12.2	119.0	15.5	167.2	-56.4	74.2	-24.5	-88.9
12.0	-11.8	108.7	15.5	137.5	-59.8	43.6	-22.9	-73.3
12.5	-11.5	96.1	15.4	107.7	-76.5	22.9	-21.9	-66.9
13.0	-11.2	83.5	15.3	77.9	-65.0	178.8	-20.1	-59.5
13.5	-11.6	73.4	15.2	49.1	-60.2	148.9	-17.4	-59.3
14.0	-12.5	64.6	15.3	20.1	-59.5	146.9	-15.1	-68.1
14.5	-13.1	57.6	15.4	-10.6	-55.2	142.1	-13.5	-81.7
15.0	-13.2	52.4	15.5	-42.1	-49.9	141.5	-12.6	-99.9
15.5	-14.1	44.8	15.5	-74.7	-45.5	117.2	-12.6	-121.4
16.0	-15.7	40.2	15.4	-108.3	-43.7	87.3	-13.9	-146.5
16.5	-18.0	39.2	15.3	-143.1	-42.0	61.2	-16.6	-177.9
17.0	-19.7	66.0	14.9	-178.3	-41.7	36.3	-21.3	136.0
17.5	-16.8	97.0	14.5	144.9	-41.5	14.5	-22.3	46.6
18.0	-12.7	96.4	13.8	105.1	-41.0	-13.7	-17.6	-12.9
18.5	-9.9	89.2	12.7	64.1	-42.1	-42.4	-15.1	-51.6
19.0	-7.1	80.6	10.3	19.1	-45.0	-76.5	-15.6	-84.5
19.5	-5.3	68.5	6.6	-19.0	-50.6	-91.9	-20.1	-107.2
20.0	-4.1	54.4	2.6	-47.9	-54.4	-69.2	-29.1	-59.0
20.5	-3.3	41.5	-0.8	-70.2	-53.6	-67.9	-19.5	-18.0
21.0	-2.8	30.8	-3.6	-89.1	-54.2	-66.0	-14.7	-29.5
21.5	-2.6	21.1	-5.8	-107.0	-54.2	-73.1	-12.0	-43.1
22.0	-2.4	11.6	-7.7	-125.3	-55.5	-89.7	-10.4	-56.0
22.5	-2.2	3.5	-9.3	-143.8	-58.9	-95.4	-9.4	-69.1
23.0	-2.2	-3.3	-10.6	-162.9	-62.1	-90.4	-8.8	-81.5
23.5	-2.1	-10.1	-11.9	176.9	-65.9	-60.7	-8.6	-92.4
24.0	-2.1	-16.9	-13.2	156.5	-62.2	-32.7	-8.6	-102.8

Typical on wafer Measurements @ 25°C

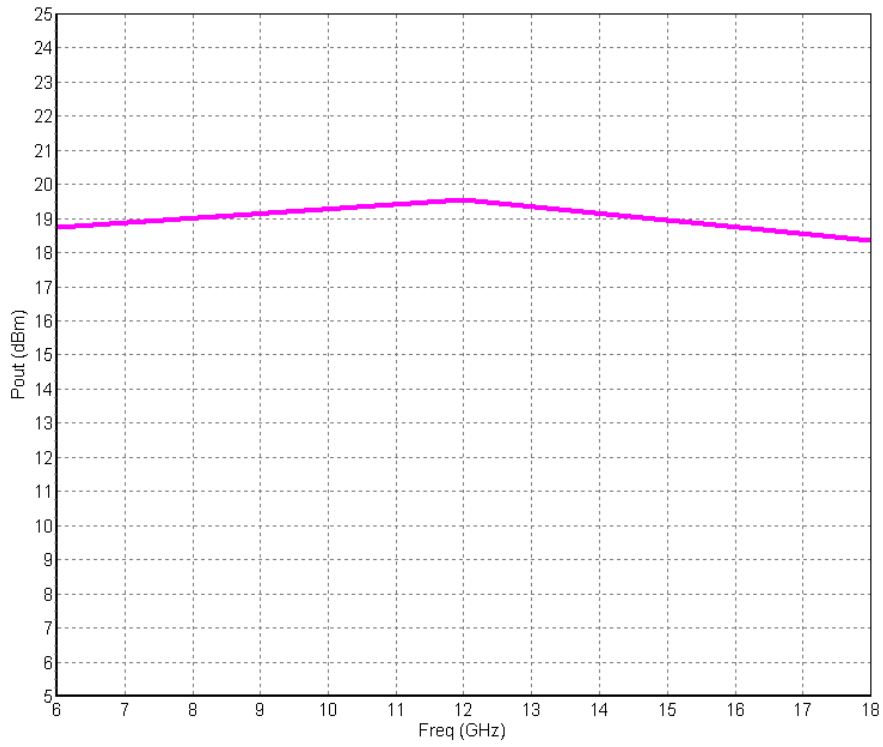
Bias conditions: $V_d = 4.5V$, V_g tuned for $I_d = 190mA$



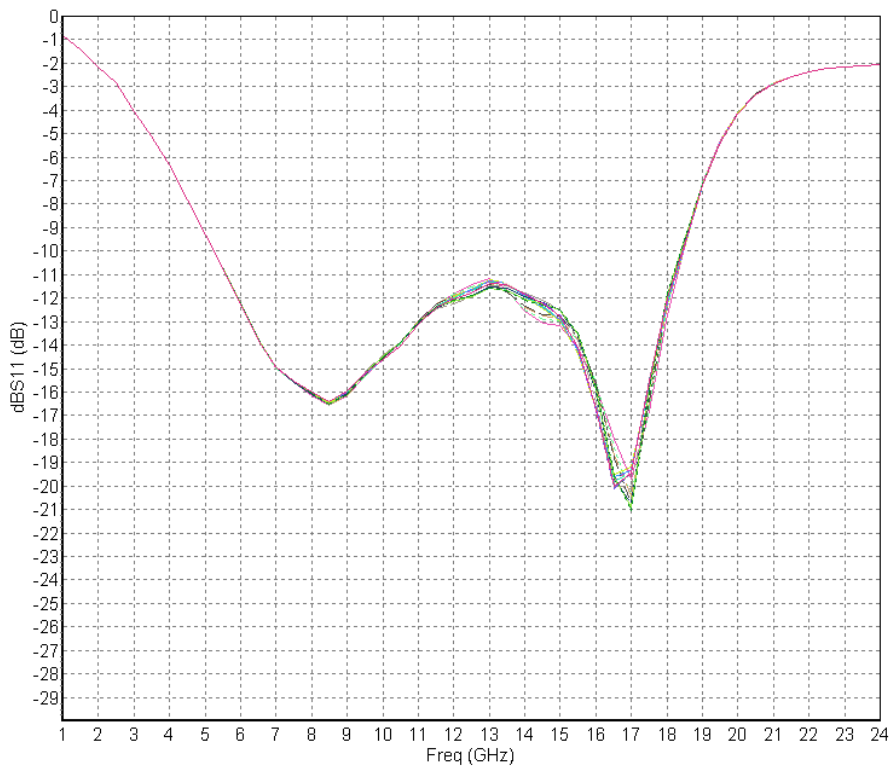
Linear Gain versus attenuator states



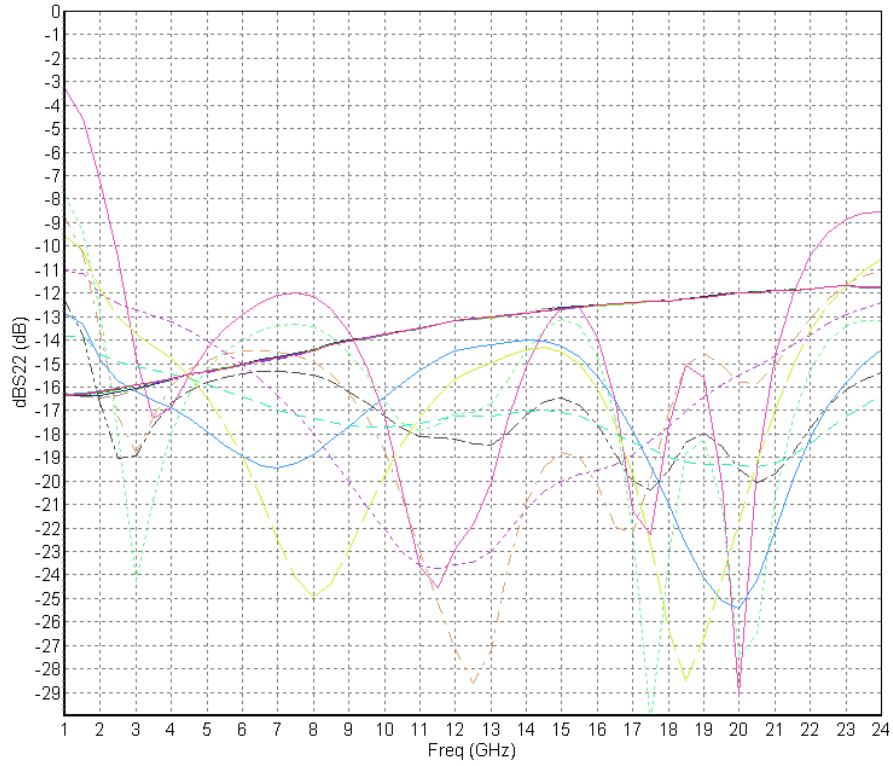
Attenuator bit values vs frequency for main states



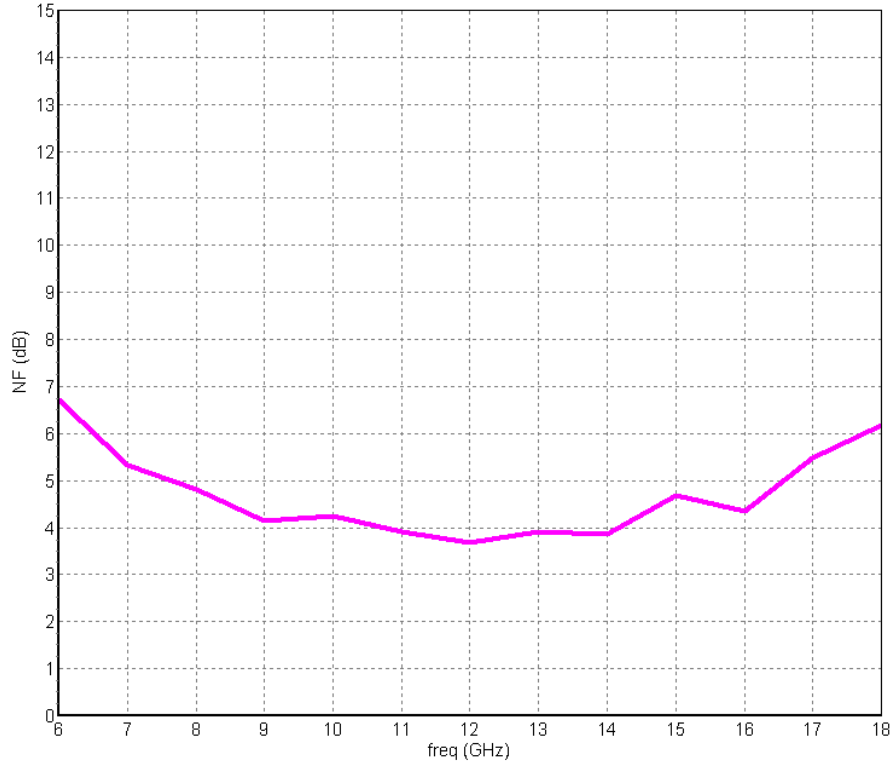
Saturated output power @ nominal state



dB(S11) versus frequency for all states



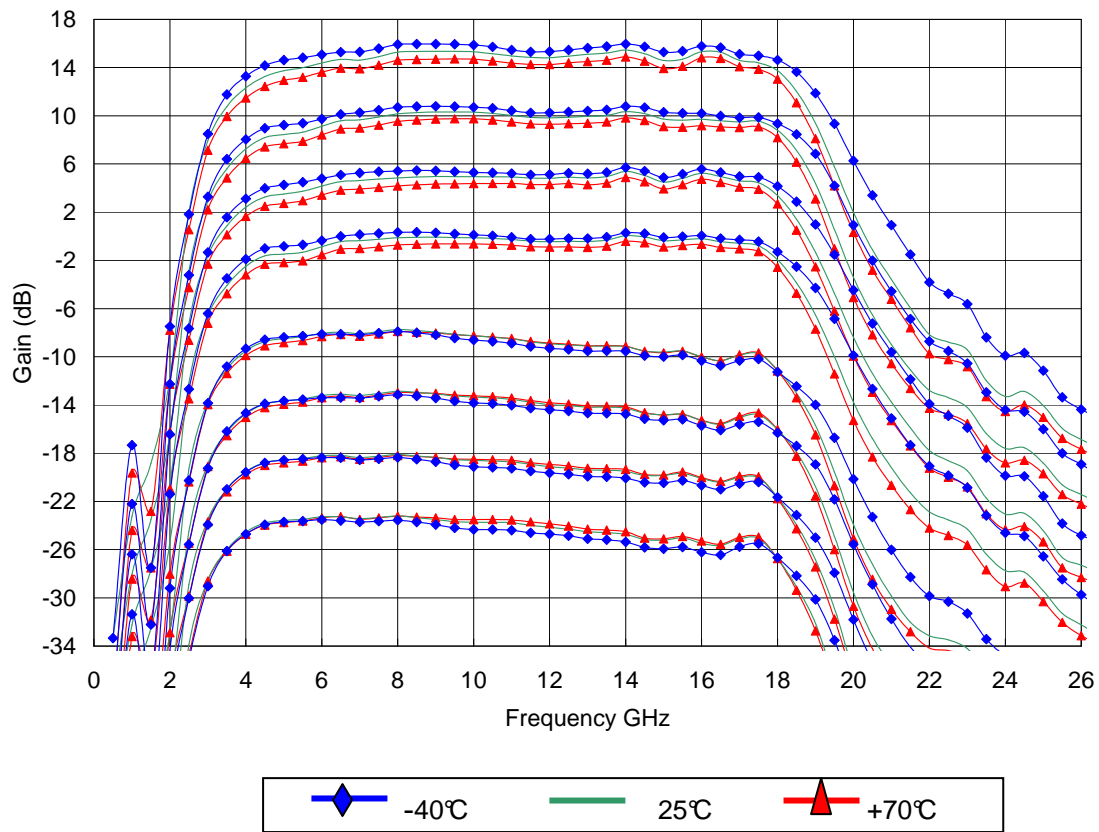
dB(S22) versus frequency for all states



Noise Figure vs frequency @ nominal state

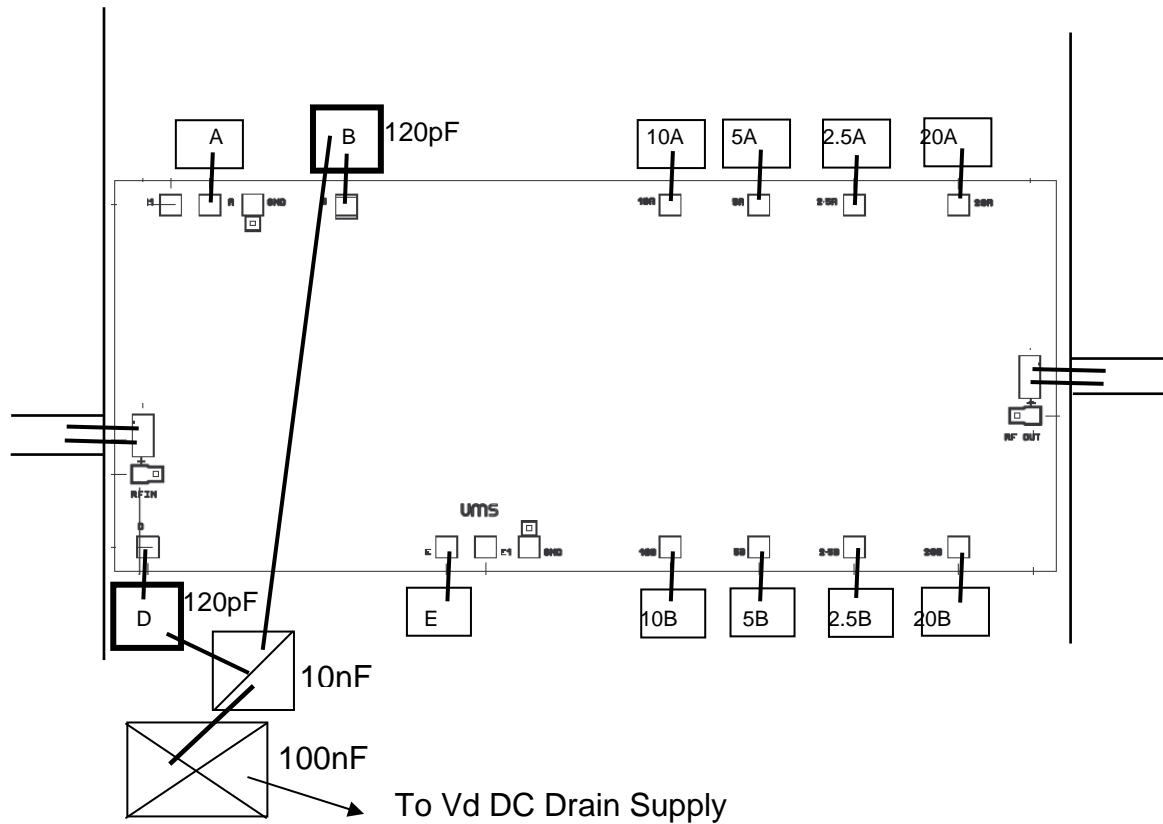
Typical test fixture Measurements

Bias conditions: $V_d=4.5V$, V_g tuned for $I_d = 190mA$



Linear Gain versus attenuation states & temperature

Chip Assembly and Mechanical Data

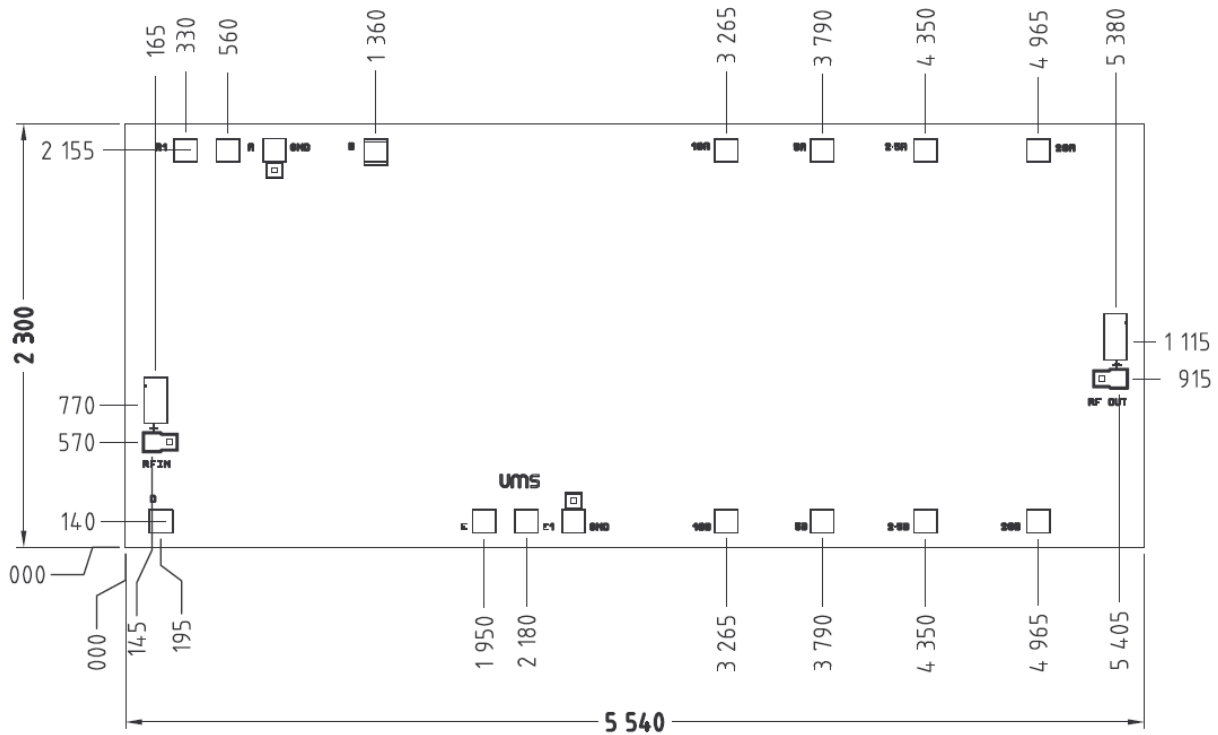


Note : Supply feed should be capacitively bypassed. 25µm diameter gold wire is to be preferred.

Recommended circuit bonding table

Label	Type	Decoupling	Comment
10A, 10B	Vc	Not required	10dB pad control
5A, 5B	Vc	Not required	5dB pad control
2.5A, 2.5B	Vc	Not required	2.5dB pad control
20A, 20B	Vc	Not required	20dB pad control
B	Vd	120pF / 10nF	Drain Supply
D	Vd	120pF / 10nF	Drain Supply
A	Vg	Not required	Gate Supply
E	Vg	Not required	Gate Supply

Bonding pad positions



UNITS : μm
Tol : $\pm 35\mu\text{m}$

Chip thickness: 100 μm

Ordering Information

Chip form : CHA3514-99F/00

Information furnished is believed to be accurate and reliable. However **United Monolithic Semiconductors S.A.S.** assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of **United Monolithic Semiconductors S.A.S.** Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. **United Monolithic Semiconductors S.A.S.** products are not authorised for use as critical components in life support devices or systems without express written approval from **United Monolithic Semiconductors S.A.S.**